CMOS MEMS – PRESENT AND FUTURE

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ABSTRACT

The paper reviews the state-of-the-art in the field of CMOS-based microelectromechanical systems (MEMS). The different CMOS MEMS fabrication approaches, pre-CMOS, intermediate-CMOS, and post-CMOS, are summarized and examples are given. Two microsystems fabricated with post-CMOS micromachining are presented, namely a mass-sensitive chemical sensor for detection of organic volatiles in air and a 10-cantilever force sensor array for application in scanning probe microscopy. The paper finishes with a look into the future, discussing key challenges and future application fields for CMOS MEMS.

INTRODUCTION

Over the last decades, CMOS (complementary metal oxide semiconductor) technology has become by far the predominant fabrication technology for integrated circuits (IC). Tremendous efforts have been made to continuously improve process yield and reliability, while minimal feature sizes and fabrication cost continue to decrease. Semiconductor roadmaps show the current state and, more important, outline the future performance of CMOS technology with ever increasing integration density and decreasing feature sizes.

Nowadays, the power of CMOS technology is not only exploited for ICs but also for a variety of microsensors and microelectromechanical systems (MEMS) benefiting from well established fabrication technologies and the availability of on-chip circuitry [1]. In recent devices, "unique selling points", such as calibration by digital programming, self-testing, and digital interfaces, have been implemented on-chip, demonstrating the strength of CMOS-based MEMS.

The paper reviews the state-of-the-art in the field of CMOS MEMS and summarizes the main technology approaches described in the literature. As examples for the "post-CMOS" approach, two CMOS-based microsystems developed at the Physical Electronics Laboratory of ETH Zurich, Switzerland are presented, (i) a mass-sensitive chemical sensor for detection of volatile organics in air, and (ii) a force sensor array for application in scanning probe microscopy. Finally, the authors take a look into the future, discussing key challenges and future application fields for CMOS MEMS and NEMS (nano electromechanical systems).

TECHNOLOGY OVERVIEW

Several classes of microsystem can be completely formed within the regular CMOS process sequence. Examples are magnetic, optical, and temperature sensors [2], which have been commercially available for many years. New magnetic sensing devices, such as inductive proximity sensors [3] and fluxgate sensors [4], have been developed by combining CMOS technology with the electrodeposition of metal coils and ferromagnetic cores, respectively.

In addition, an increasing number of microelectromechanical systems (MEMS) have been produced using CMOS (and BiCMOS) technology in combination with compatible micromachining and thin film deposition steps. The additional fabrication steps can precede (*pre*-CMOS) or follow (*post*-CMOS) the regular CMOS process, or can be performed in-between the regular CMOS steps (*intermediate*-CMOS).

In the *pre-CMOS* approach, the MEMS structures or part of them are formed before the regular CMOS process sequence. Examples are vertical Hall devices based on a pre-CMOS trench etching technology [5], "embedded" polysilicon microstructures based on the iMEMS technology of Sandia National Laboratories [6], and pre-CMOS silicon fusion bonding [7]. In all cases, the pre-micromachined wafers have to meet stringent criteria, e.g., with respect to contaminations, to be able to enter a microelectronics processing line afterwards.

In the *intermediate-CMOS* approach, the CMOS process sequence is interrupted for additional thin film deposition or micromachining steps. This approach is commonly exploited to implement surface micromachined polysilicon structures [8] in CMOS technology. Either the standard gate polysilicon or an additional low-stress polysilicon layer are used as structural material. Exam-

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ples of commercially available microsensors relying on intermediate process steps are Infineon's pressure sensor IC [9] and Analog Devices' accelerometers [10]. Both are based on BiCMOS technologies, use polysilicon structures as micromechanical elements, and release the MEMS by sacrificial layer etching.

In the *post-CMOS* approach, two general fabrication strategies can be distinguished. In the first strategy, the MEMS structures are completely built on top of a finished CMOS substrate, leaving the CMOS layers untouched. Examples for this approach are Texas Instruments' Digital Micromirror Device (DMD, [11]), the electroplated ring gyroscope [12,13] developed by the University of Michigan and Delphi Automotive Systems, the electroplated acceleration switch developed by Infineon and the University of Bremen [14], and Honeywell's thermal imagers [15]. In all four cases, the microstructures are released using sacrificial layer etching. Recently, a biosensor relying on disposable cartridges with CMOS-based microelectrode sensor arrays has been demonstrated at Stanford University [16] using a similar "additive" fabrication approach. Even though the fabrication process does not require any micromachining steps, the gold electrodes and chip passivation required for biocompatibility are deposited on top of the completed CMOS substrate. Another recent CMOS MEMS approach demonstrated by *austriamicrosystems* combines a sensor wafer with a CMOS substrate wafer: a capacitive acceleration sensor is fabricated by wafer-bonding the sensor wafer with polysilicon sensor structures on to a CMOS substrate wafer with sensing electrode and read-out electronics [17].

Alternatively, the MEMS can be obtained by machining the CMOS layers after the completion of the regular CMOS process sequence. Using a variety of CMOS-compatible bulk- and surface-micromachining techniques [18-24], e.g., pressure [25-27], inertial [28], flow [29], chemical [1,30-32], and infrared radiation [33,34] sensors have been produced this way.

Both post-CMOS approaches are attractive, because the CMOS wafers can be processed at any CMOS (or BiCMOS) foundry. This way, even very advanced CMOS technologies with multiple (copper) metallizations can be exploited for MEMS [35]. The main limitation of the post-CMOS technologies is the stringent thermal budget for the add-on fabrication steps, limiting process temperatures to about 400 °C.

POST-CMOS MEMS & NEMS

The post-CMOS approach relying on anisotropic etching of silicon from the back of the wafer is pursued at the Physical Electronics Laboratory (PEL) of ETH Zurich, Switzerland, and will be discussed in more detail in the following.

After completion of the industrial CMOS process, membrane-type structures for, e.g., thermal insulation of microsensors, are released by anisotropic etching from the back of the wafer using a potassium hydroxide (KOH) solution. Crucial for the etching result is the quality of the back surface of the CMOS wafers and the initial oxygen concentration of the wafer starting material [19,36].

Membranes consisting of the dielectric CMOS layers on top of the silicon substrate are obtained by etching through the complete bulk silicon of the CMOS wafer. In this case, the thermal oxide serves as an "intrinsic" etch-stop layer. The resulting dielectric membrane structures are used for sensors requiring excellent thermal insulation, such as infrared radiation or calorimetric chemical sensors. Polysilicon and metal structures sandwiched in-between the dielectric layers can be used to create, e.g., thermopiles and heating resistors. As an example, Fig. 1 shows a 256-pixel thermal imager [34] with four on-chip low-noise amplifiers. All 256 pixels are located on a single, 5 mm by 5 mm membrane consisting of the dielectric layers of the CMOS process. Electroplated gold lines thermally separate neighboring pixels and stabilize the membrane. Each pixel contains an integrated thermopile to measure the temperature elevation generated by the absorbed IR radiation.

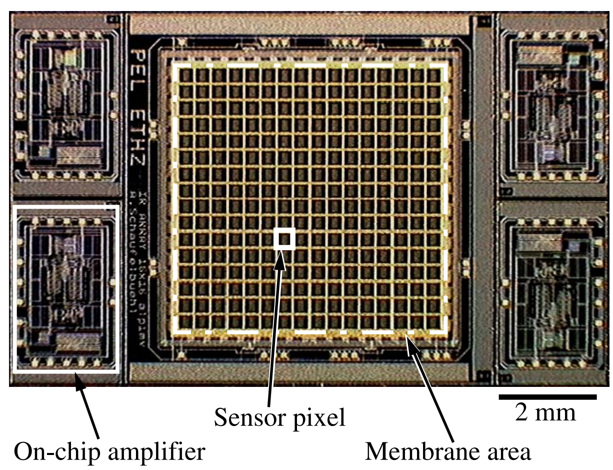

Figure 1: 256-pixel thermoelectric IR sensor array with four on-chip low-noise amplifiers [34] fabricated with a 1 μm CMOS technology of EM Microelectronic-Marin, Switzerland.

Silicon membranes and suspended n-well island structures are released by combining the KOH etching step with an electrochemical etch-stop technique. In this case, the etching stops at the pn-junction between the CMOS n-well and the p-type substrate. During the etching step performed with a four-electrode set-up, etching potentials must be applied to the structural n-wells and the substrate. The etching potentials are applied with spring-loaded contacts to large contact pads on the CMOS wafer. From there, the etching potentials are routed to the individual n-well structures through a special metal network inside the scribe line. The special preparation sequence for the electrochemical etching of CMOS wafers is described in [19]. By combining the bulk-micromachining process with additional reactive-ion-etching (RIE), not only membrane structures, but also bridges and cantilever beams can be released.

Depending on the actual microsystem, additional thin film deposition steps (e.g., electroplating of metals or deposition of polymer layers) might complement the process sequence.

In the following, two CMOS-based microsystems developed recently at the PEL and processed at *austriamicrosystems* (AMS), Unterpremstätten, Austria are presented:

- CMOS *mass-sensitive chemical microsystem* for detection of volatile organic compounds in air
- CMOS *force sensor array* for application in scanning probe microscopy (SPM)

Mass-Sensitive Chemical Microsensor

Fig. 2 shows a photograph of the CMOS-based mass-sensitive chemical sensor for detection of volatile organic compounds in air [37]. Key element of the microsystem is a 150 μm by 150 μm silicon cantilever beam. Integrated heating resistors and four piezoresistors arranged in a Wheatstone bridge configuration allow for electrothermal excitation and piezoresistive detection of transverse cantilever vibrations. Alternatively, magnetic excitation and MOSFET-based detection of vibrations can be used [38].

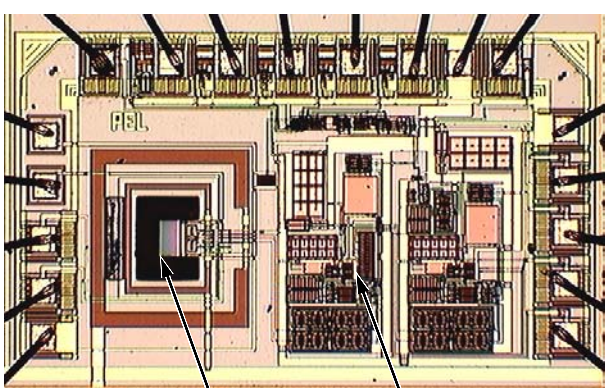

Figure 2: Mass-sensitive chemical sensor system consisting of polymer-coated cantilever beam and on-chip amplifying feedback circuit to operate the cantilever at its resonance frequency [37].

The cantilever is coated with a polymer as chemically sensitive layer. Upon absorption of analyte molecules in the polymer layer, its mass increases and the fundamental resonance frequency of the cantilever structure decreases. The cantilever's resonance frequency is recorded by incorporating it in an on-chip amplifying feedback circuit (see schematic in Fig. 3). Using the bandpass characteristic of the cantilever with its high Q-factor, the cantilever acts as the frequency-determining element in the feedback loop.

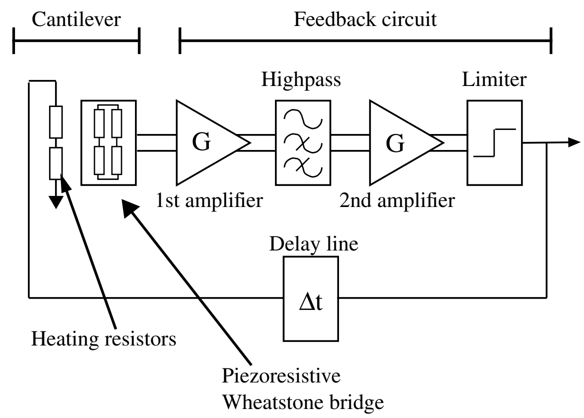

Figure 3: Block diagram of the mass-sensitive chemical sensor system [37].

The chemical microsystem has been fabricated using a 0.8 μm CMOS technology of AMS. The silicon cantilever consisting of the CMOS n-well with CMOS dielectric layers on top is released by anisotropic silicon etching with an electrochemical etch-stop technique in combination with reactive ion etching. In a final process step, the cantilever is spray-coated with the chemically sensitive polymer.

Without polymer, the cantilever beam has a resonance frequency of approximately 400 kHz and a Q-factor of 950 in air [37]. Fig. 4 shows the frequency stability and corresponding limit of detection for octane of a cantilever coated with poly(etherurethane) (PEUT) as a function of the polymer thickness. The short-term frequency stability of the microsystem is approx. 0.03 Hz for polymer thicknesses smaller than 4 μm [37]. For thicker polymer layers, the frequency stability is reduced due to the reduced quality factor. The detection limit for octane is approx. 1 ppm for polymer thicknesses between 2 and 4 μm. For smaller polymer thickness, the lower mass increase due to the small polymer volume reduces the resolution.

The mass-sensitive chemical microsystem is part of a handheld application-specific chemical microsystem presented in [31,32].

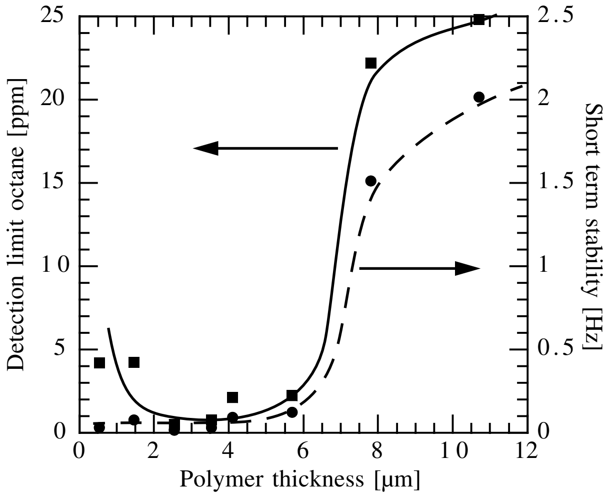

Figure 4: Frequency stability and corresponding limit of detection for octane as a function of the polymer thickness for a poly(etherurethane)-coated cantilever. The lines are guides to the eye only [37].

Force Sensor Array

Fig. 5 shows an array of ten force sensors for application in Atomic Force Microscopy (AFM) [39]. The system combines, on a single chip, ten cantilevers with integrated thermal actuators, piezoresistive sensors, and driving and signal conditioning circuitry. Alternatively, force sensor arrays with MOSFET-based strain gauges for deflection detection have been investigated [40]. The cantilevers in Fig. 5 have a pitch of 110 µm yielding an array with a total span of 1.1 mm. Each cantilever is 500 µm long and 85 µm wide. The total dimensions of the sensor die are 2.1 mm by 4 mm.

The force sensor array has been fabricated using a 2.0 µm CMOS process of AMS. The cantilevers are released by anisotropic etching with an electrochemical etch-stop technique in combination with wet and reactive ion etching [39]. The resulting cantilevers consist of the silicon n-well and the dielectric layers of the CMOS process. Silicon tips can be fabricated at the cantilever ends by anisotropic silicon etching using TMAH [41].

Constant force images and force-distance curves were recorded with the cantilever array without the need of an external optical read-out or a z-axis piezotube. The cantilever deflections are controlled with an external electronic feedback loop. The cantilever under operation is selected with the on-chip multiplexer (see block diagram in Fig. 6). The external controller applies a proper heating power via an on-chip buffer amplifier to the thermal actuator in order to maintain constant cantilever deflection. The piezoresistive output signal, which is proportional to the cantilever deflection, is amplified on-chip and applied to the external controller, closing the feedback loop.

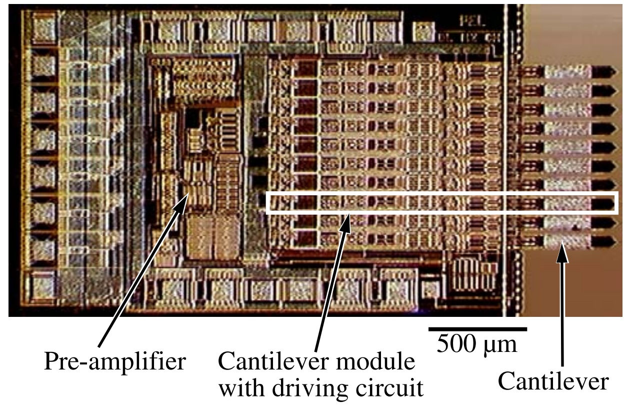

Figure 5: Photograph of a processed AFM probe with an array of ten cantilevers and on-chip driving and signal conditioning circuitry [39].

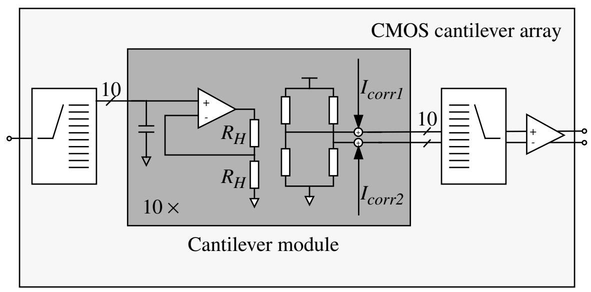

Figure 6: Block diagram of the 10-cantilever force sensor nanosystem [39].

When the deflection of a single cantilever is regulated, it is crucial that all other cantilevers of the array remain at their position. For this reason, each cantilever module contains a sample-and-hold block, which maintains the voltage across the heating resistors until the individual cantilever is active again. The integrated system is designed to operate at a multiplexing frequency of 10 kHz, i.e., an operation time of 100 µs per cantilever.

The cantilevers have a spring constant of about 1 N/m [39]. The thermal bimorph actuator has an efficiency of 0.7 µm/mW. Images spanning an area of 1.1 mm by 110 µm were recorded in constant force mode (see Fig. 7). The vertical resolution of the force sensor array is about 3 nm.

Figure 7: Large area constant force image collected with the 10-cantilever array. The horizontal and vertical ranges are 1.1 mm and 110 µm, respectively. The letters are formed by 600 nm aluminum covered with silicon oxide and nitride [39].

QUO VADIS CMOS MEMS?

Where will CMOS MEMS go from here? Will there be a "next" technology that may eventually replace CMOS MEMS? Our look into the crystal ball produced four concurrent directions:

- CMOS MEMS based products
- CMOS NEMS as platform for nano
- CMOS MEMS based BIOTRONICS
- Siliconless CMOS MEMS

CMOS MEMS Based Products

We expect a consolidation of current CMOS MEMS research to result in further products beyond the currently dominating pressure sensors and accelerometers for automotive applications.

A relative newcomer is the gas flow sensor ASF-1400 developed by Sensirion, Switzerland [42] based on a micromachined CMOS thermal flow sensor chip developed at our laboratory [29].

Further product families may mushroom based on the following trends:

- Exploitation of laboratory CMOS MEMS by systematic process development for industrial mass production [17].
- Co-integration of more sophisticated circuits including digital interfaces and micro controllers with the microstructures [25]: the part that makes the microsystem smart will become more powerful and less expensive.
- Development of packaging to protect the vulnerable CMOS chip from environmental impact, but allow for interaction with physical and chemical measurands [43]. There is not only the need of a "package for MEMS", but there is also "MEMS for packaging", i. e., MEMS supporting packaging techniques [44].

CMOS NEMS as Platform for Nano

Current nanotechnology research programs involve many disciplines concerned with structures in the nanometer range: materials, coatings, and biological, as well as fluidic components and nanoelectromechanical systems (NEMS). The latter comprise mechanical structures that have nanometer dimensions or manipulate matter at this level. The name suggests an evolutionary process from MEMS. Nanosystems leaving the laboratory and having an impact on the market must deliver not only the basic device function, but must also be robust and stable. A number of challenges have to be faced:

- **The interconnect challenge.** More than nine orders of magnitude have to be bridged between the human handling of the system and the nano structures under investigation. We can possibly span this range in three steps. Humans are capable to handle mm-sized objects. These in turn may contain micrometer-sized features, which allow to connect to the nanometer scale. In addition, signals in these structures may be generated by only a few electrons, and hence, profit from integrated signal conditioning. It is therefore important to realize that "micro" is often an important, if not indispensable, carrier for "nano", and a sharp distinction between MEMS and NEMS may be futile.
- **The 300 K question.** NEMS have been used for exciting scientific experiments, most of which carried out in what engineers consider "exotic" environments like very low temperature and ultra-high vacuum of little, if any interest for mass product applications. How can NEMS be operated outside the lab? For example, oscillations of a resonator operated under laboratory conditions may be strongly influenced by surface effects and internal friction. In contrast, a resonant cantilever as a gas sensor operated at room temperature and in air experiences viscous and acoustic damping and, thus, needs a different kind of optimization, and notably judiciously chosen driving and signal conditioning circuitry.

- **Everything nano?** A benefit of nanosystems is their high sensitivity to effects caused by the measurand. But this in turn creates a problem because such systems are highly susceptible to disturbing external influences. Miniaturization is not a value by itself: the application determines the proper size of the system; economics also holds for nanosystems. The semiconductor industry demonstrates in an impressive fashion how capital spending explodes with imploding device dimensions. From this point of view it makes sense to focus on the crucial nano part and do the rest of the system using microtechnology including microelectronics. In this sense, we expect to see NEMS integrated in MEMS, notably CMOS MEMS.

We believe that CMOS-compatible micromachining can provide essential support to overcome these obstacles. IC technology has much to offer to the micro and nano system designer, especially the vast fabrication experience gained over the last decades and the optimized reliability and yield of industrial IC processes. Another advantage is the existence of many circuit design libraries. The connection to CMOS technology opens the door to batch fabrication of e. g. arrays of devices. The CMOS and micromachining combination has been developed over the last 10 years and is now employed by several CMOS manufacturers. Meanwhile, industrial CMOS processing has become a nanoscience itself. The structures currently fabricated (most prominently the gate oxide thicknesses and the gate length) have reached the nano-level.

CMOS MEMS Based Micro Biotronics

MICRO BIOTRONICS is part of the wider vision [45] of merging BIO, which stands for the life sciences in a broad sense including biology, biochemistry, biomedical science, pharmacology, and food science, with TRONICS, which stands for the (miniaturized) hardware: micro and nano electronics and mechanics, as well as mechatronics and micro fluidics with its transducers and circuits. Thus micro biotronics in particular includes micro-bio-electronics and micro-bio-mechatronics.

BIO MEMS or BIO MST denote the tools, by which MEMS or MST technologies are merged with life-related materials and functions. On the device level, this leads to biophysical or biochemical microdevices and microsystems. Examples for biotronic devices are biochemical sensors, parallel-scanning biochemical atomic force microscopes with bio-functional tips, bio-mimetic devices and their materials, or integrated circuits merged with MEMS or NEMS and living cells.

One challenge is that the BIO part requires operation in water abhorred by microelectronics. Living cells such as brain cells wired up with integrated circuitry have to be kept alive by, e. g., a microfluidic supply system. Another challenge is stability, yet another the interface between biological and electronic materials and devices. This can be illustrated by biotronic sensors, electronic devices that transfer chemical, biological, or biomedical signals to electronic signals by combining electronic devices with biosensitive materials. Examples are immuno assays, enzyme-based catalytic sensors, phospholipid membrane sensors, sensors employing living cells, or even sensors using insect antennae. Specific examples are:

- Force sensor arrays with different functionalized tips on a CMOS chip with driving and signal conditioning and acquisition circuits for e.g. multiple immuno assays.
- MEMS for surgical sewing and gluing microrobots with sensory feedback used in minimal invasive surgery.
- NEURO MEMS for neuroelectronic interfacing with synaptically connected neurons immobilized on a semiconductor chip for e. g. stimulation and recording of neural activities.
- Biochemical sensors, i.e. devices which might address molecules on the subnano-molar level as well as single molecules and single cells, for medical diagnosis, food production and quality control, security and environmental control.
- Bioassays for high-throughput screening making use of interactions between peptides, RNA, DNA, and enzymes.

Severe limitations of the BIO part have to be overcome in order to obtain reliable BIO MEMS: the limited lifetime of enzymes and antibodies, the limited ruggedness of lipid bilayers or whole cells, reduced performance of receptors by immobilization on a surface, reduced performance of host compounds by synthetic matrices. The ultimate quest is to combine chemical and biological receptors with advanced detecting systems (e.g. microcalorimeters, dielectric probes, impedance analysis, and mass sensitive devices), also on the mesoscopic level by using chemically modified AFM cantilever tips.

Siliconless CMOS MEMS

The strength of silicon IC technologies shows only if the number of parts is high. Thus, from a fabrication-cost point of view, CMOS MEMS is cost-effective for MEMS-based mass products or product families exploiting the same chip or process. Silicon manufacturing may be to expensive for applications involving small numbers of parts, even when we take into account that chip cost is only one constituent of the overall fabrication cost besides packaging and testing.

Gas microsensors as described above use polymer layers merged with silicon-based MEMS. Could we make the whole microsystem out of polymers? Microstructures can indeed be made using plastic or glass, but what about the crucial on-chip signal conditioning? Thin film transistors fabricated by ink-jet printing [46] and organic circuits on flexible polymeric substrates [47] have been demonstrated recently. Thus we may be allowed to speculate that siliconless MEMS based on organic materials may become feasible, at least with the bare minimum of on-chip circuits required to drive a transducer or to extract a signal. These organic MEMS can then be connected to standard, inexpensive mass-product-type silicon chips for further signal processing and "smartness".

Hybrid or monolithic?

In the case of microsensors, S. Middelhoek distinguished two approaches which involve silicon to a different extent [48]:

(1) A sensor made with various sophisticated processes is combined with a separate standard integrated circuit (hybrid approach).

(2) A sensor made in IC compatible technology is combined with sophisticated circuits to compensate for sensor deficiencies on the same chip (monolithic approach; this is the way of CMOS MEMS).

We are not sure, whether organic MEMS goes back to the first approach or will constitute a third way: a simple sensor with a minimum of organic circuitry is combined with standard (and therefore low-cost) integrated circuits. The future will show.

When should a monolithic integration be preferred over a hybrid approach and vice versa? This question has to be answered from an economic point of view for every microsystem case by case. In general, high-volume applications in the automotive and consumer electronics industry benefit from monolithic integration. Moreover, array-type sensors, such as thermal imagers, require co-integration of at least addressing circuitry in order to reduce the number of electrical interconnects [49].

The fabrication cost of the dice, be it monolithically integrated or in a hybrid approach, is however only one component of the total cost. Packaging and testing are major, if not dominating, cost components in microsystem production and must be considered from the very beginning of the system design.

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